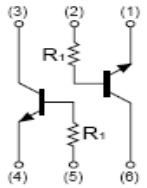
UMH4N

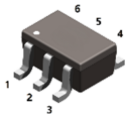
Dual Digital Transistor(NPN+NPN)

Features

- Two DTC114T transistors are built-in a package
- Transistor elements are independent, eliminating interference
- Mounting cost and area can be cut in half



R1=10KΩ



SOT-363

Mechanical Data

- Case: SOT-363
- Molding Compound: UL Flammability Classification Rating 94V-0
- Terminals: Matte tin-plated leads; solderability-per MIL-STD-202, Method 208

Ordering Information

Part Number	Package	Shipping Quantity	Marking Code
UMH4N	SOT-363	3000 pcs / Tape & Reel	H4

Maximum Ratings (@ T_A = 25°C unless otherwise specified)

Parameter	Symbol	Value	Unit
Collector-Base Voltage	V_{CBO}	50	V
Collector-Emitter Voltage	V_{CEO}	50	V
Emitter-Base Voltage	V_{EBO}	5	V
Collector Current	I_C	100	mA

Thermal Characteristics

Parameter	Symbol	Value	Unit
Power Dissipation	P_D	150	mW
Thermal Resistance Junction-to-Air	$R_{\theta JA}$	833	°C/W
Operating Junction Temperature Range	T_J	-55 ~ +150	°C
Storage Temperature Range	T_{STG}	-55 ~ +150	°C

Electrical Characteristics (@ T_A = 25°C unless otherwise specified)

Parameter	Symbol	Test Condition	Min.	Typ.	Max.	Unit
Collector-Base Breakdown Voltage	$V_{(BR)CBO}$	I_C = 50μA, I_E = 0	50	-	-	V
Collector-Emitter Breakdown Voltage	$V_{(BR)CEO}$	I_C = 1mA, I_B = 0	50	-	-	V
Emitter-Base Breakdown Voltage	$V_{(BR)EBO}$	I_E = 50μA, I_C = 0	5	-	-	V
Collector Cut-off Current	I_{CBO}	V_{CB} = 50V, I_E = 0	-	-	0.5	μA
Emitter Cut-off Current	I_{EBO}	V_{CB} = 4V, I_C = 0	-	-	0.5	μA
DC Current Gain	h_{FE}	V_{CE} = 5V, I_C = 1mA	100	-	600	-
Collector-emitter Saturation Voltage	$V_{CE(sat)}$	I_C = 10mA, I_B = 1mA	-	-	0.3	V
Transition Frequency	f_T	I_C = 5mA, V_{CE} = 10V f = 100MHz	-	250	-	MHz
Input Capacitance	R_1		7	10	13	kΩ

Ratings and Characteristic Curves (@ T_A = 25°C unless otherwise specified)

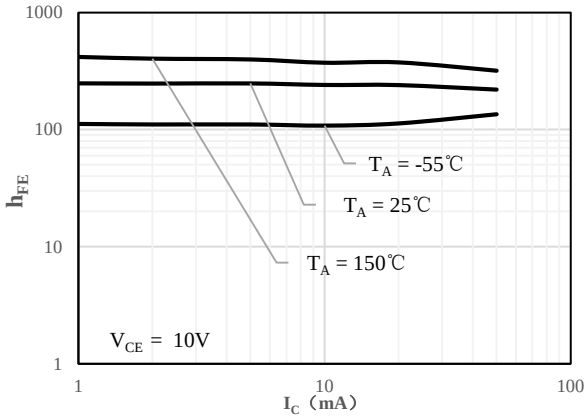


Fig 1 h_{FE} vs. I_C

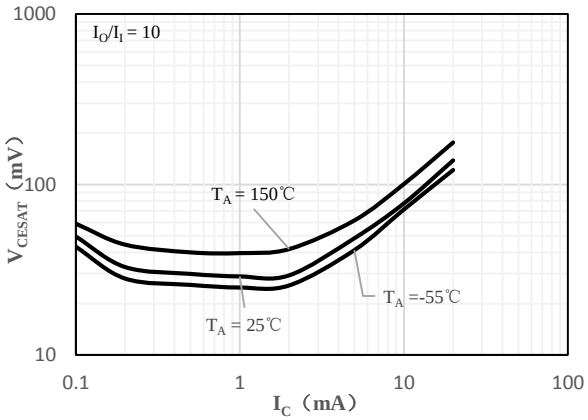


Fig 2 $V_{CE(sat)}$ vs. I_C

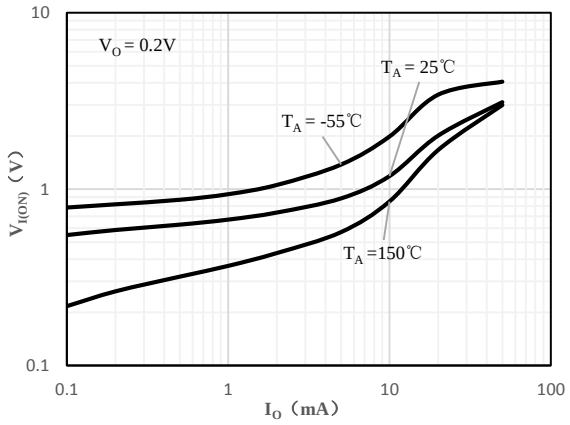


Fig 3 Input Voltage vs Output Current

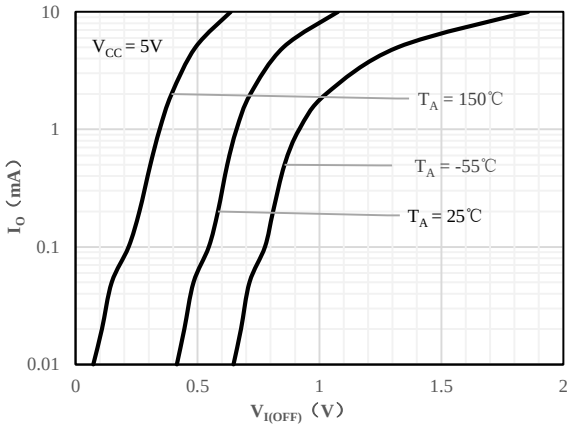


Fig 4 Output Current vs Input Voltage

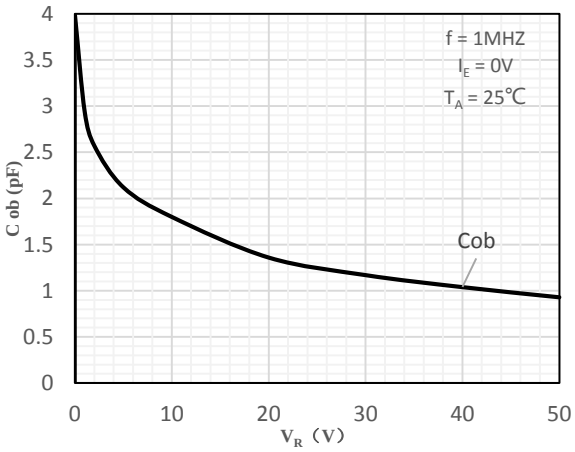


Fig 5 Output Capacitance

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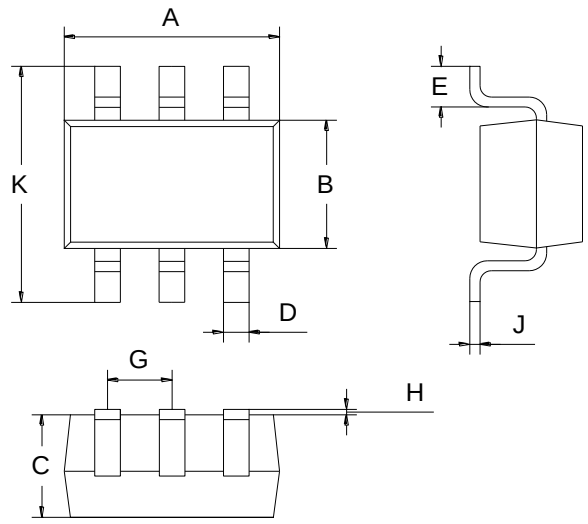
Dual Digital Transistor(NPN+NPN)

Package Outline Dimensions (Unit: mm)



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Dimension	**Min.**	**Max.**
A	2.00	2.20
B	1.15	1.35
C	0.85	1.05
D	0.15	0.35
E	0.25	0.40
G	0.60	0.70
H	0.02	0.10
J	0.05	0.15
K	2.20	2.40

Mounting Pad Layout (Unit: mm)

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