

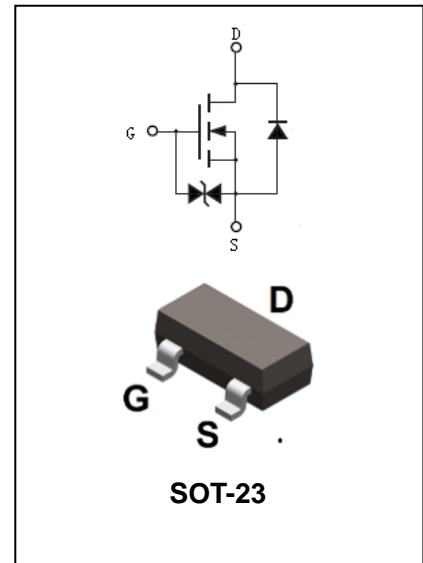


### FEATURES

- High density cell design for low  $R_{DS(ON)}$
- Voltage controlled small signal switch
- Rugged and reliable
- High saturation current capability

### APPLICATIONS

- N-channel enhancement mode effect transistor
- Switching application



### ORDERING INFORMATION

Type No.	Marking	Package Code
LGE05N60C	05N60	SOT-23

### MAXIMUM RATING @ $T_a=25^\circ\text{C}$ unless otherwise specified

Symbol	Parameter	Value	Units
$V_{DSS}$	Drain-Source voltage	60	V
$V_{DGR}$	Drain-Gate voltage( $R_{GS} \leq 1\text{M}\Omega$ )	60	V
$V_{GSS}$	Gate -Source voltage - continuous -Non Repetitive ( $t_p < 50\mu\text{s}$ )	$\pm 20$ $\pm 40$	V
$I_D$	Maximum Drain current -continuous -Pulsed	600 1600	mA
$P_D$	Power Dissipation	350	mW
$R_{\theta JA}$ (NOTE1)	Thermal resistance, Junction-to-Ambient	357	$^\circ\text{C}/\text{W}$
$R_{\theta JC}$ (NOTE1)	Thermal resistance, Junction-to-Case	90	$^\circ\text{C}/\text{W}$
$T_J, T_{stg}$	Junction and Storage Temperature	-50 to +150	$^\circ\text{C}$

NOTE1:  $R_{\theta JA}$  is the sum of the junction-to-case and case-to-ambient thermal resistance where the case thermal reference is defined as the solder mounting surface of the drain pins.  $R_{\theta JC}$  is guaranteed by design while  $R_{\theta CA}$  is determined by the user's board design. The value of  $R_{\theta JA}$  is measured with device mounted on 1 in2 FR-4 board with 2 oz copper.



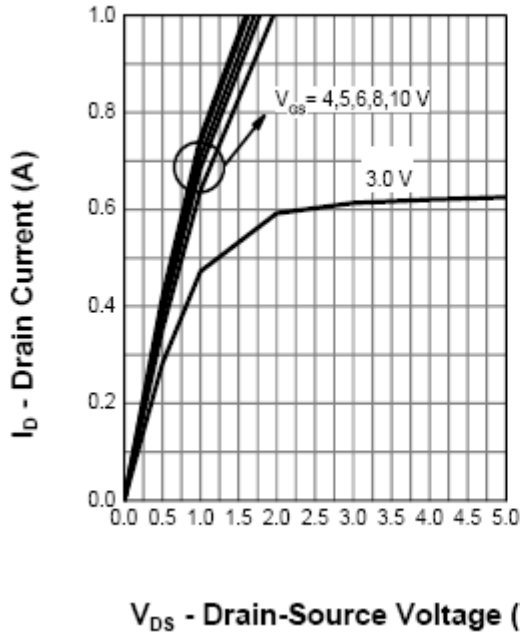
### ELECTRICAL CHARACTERISTICS @ Ta=25°C unless otherwise specified

Parameter	Symbol	Test conditions	MIN	TYP	MAX	UNIT
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS}=0V, I_D=10\mu A$	60	70	-	V
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\mu A$	1	-	2.0	V
Gate-body Leakage	$I_{GSS}$	Forward $V_{DS}=0V, V_{GS}=20V$	-	-	1	$\mu A$
		Reverse $V_{DS}=0V, V_{GS}=-20V$	-	-	-1	
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS}=60V, V_{GS}=0V$	-	-	1	$\mu A$
		$V_{DS}=60V, V_{GS}=0V, T_j=125^\circ C$	-	-	500	
On-state Drain Current	$I_{D(on)}$	$V_{GS}=10V, V_{DS} \geq 2.0V_{DSS(on)}$	0.5	1.0	-	A
Drain-Source on-voltage	$V_{DS(on)}$	$V_{GS}=10V, I_D=500mA$	-	0.6	3.75	V
		$V_{GS}=5V, I_D=50mA$	-	0.09	1.5	
Forward transconductance	$g_{FS}$	$V_{DS}=10V, I_D=200mA$	80	-	-	mS
Static drain-Source on-resistance	$R_{DS(on)}$	$V_{GS}=10V, I_D=500mA,$	-	-	1.7	$\Omega$
		$V_{GS}=5.0V, I_D=50mA$	-	-	2.5	
On-state drain current	$I_{D(on)}$	$V_{GS}=10V, V_{DS}=7.5V$	0.5	1.0	-	A
Drain-Source diode forward voltage	$V_{SD}$	$V_{GS}=0V, I_S=115mA$	-	0.88	1.2	V
Input capacitance	$C_{ISS}$	$V_{DS}=25V, V_{GS}=0V, f=1.0MHz$	-	20	50	$pF$
Output capacitance	$C_{OSS}$		-	11	25	
Reverse transfer capacitance	$C_{RSS}$		-	2	5	
Turn-On Delay Time	$t_{D(on)}$	$V_{DD} = 30V, I_D = 0.2A,$ $R_L = 150\Omega, V_{GS} = 10V,$ $R_{GEN} = 25\Omega$	-	6	-	ns
Turn-On rise Time	$t_r$		-	5	-	
Turn-Off Delay Time	$t_{D(off)}$		-	25	-	
Turn-Off Fall Time	$t_f$		-	15	-	

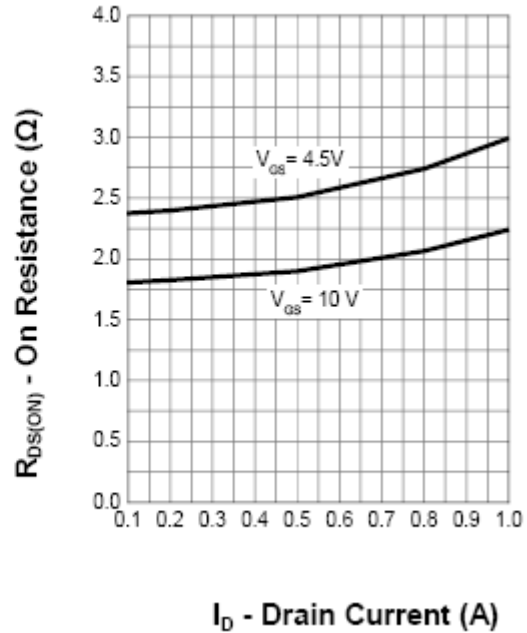


TYPICAL CHARACTERISTICS @ Ta=25°C unless otherwise specified

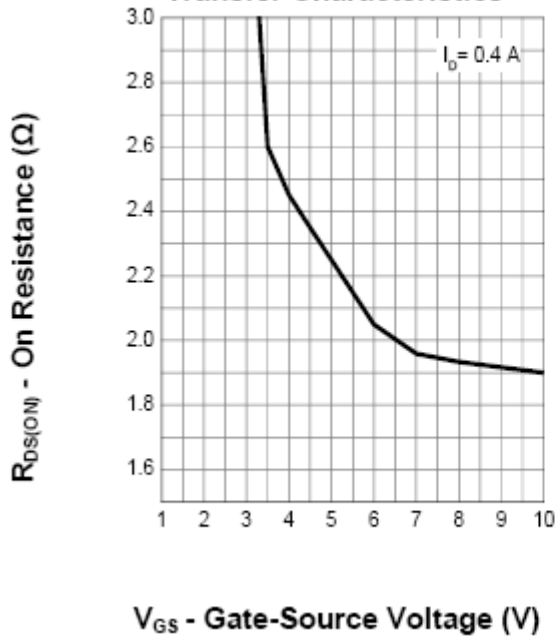
**Output Characteristics**



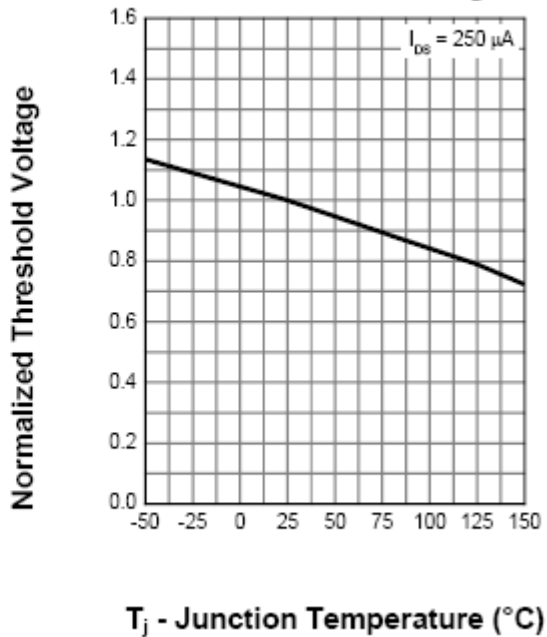
**Drain-Source On Resistance**



**Transfer Characteristics**

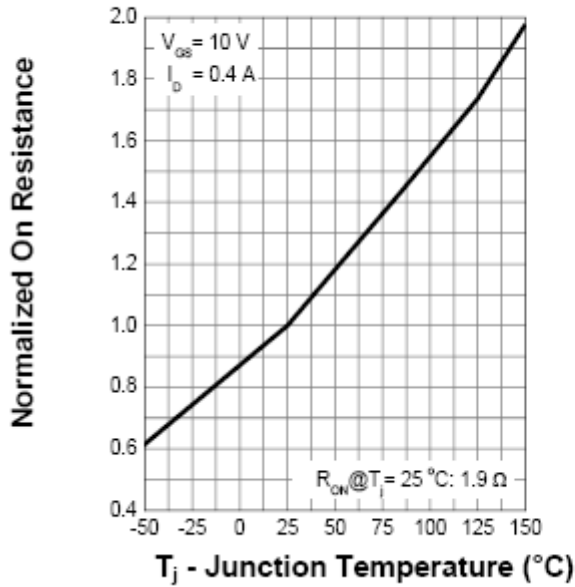


**Gate Threshold Voltage**

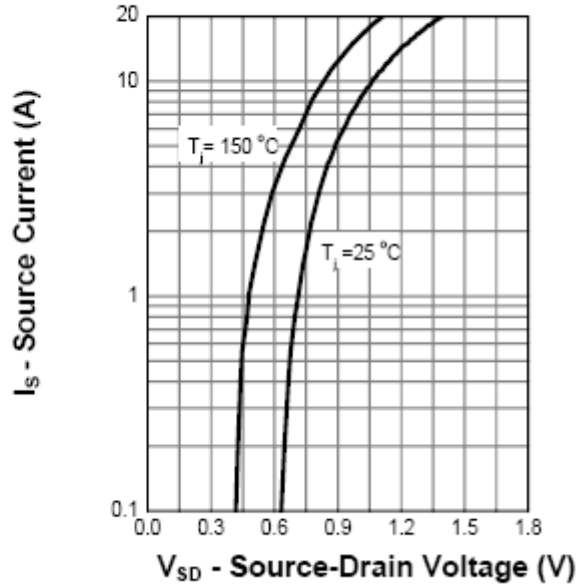




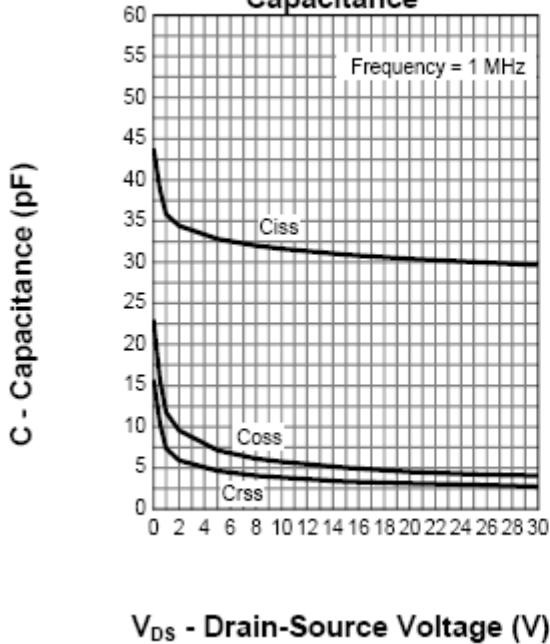
### Drain-Source On Resistance



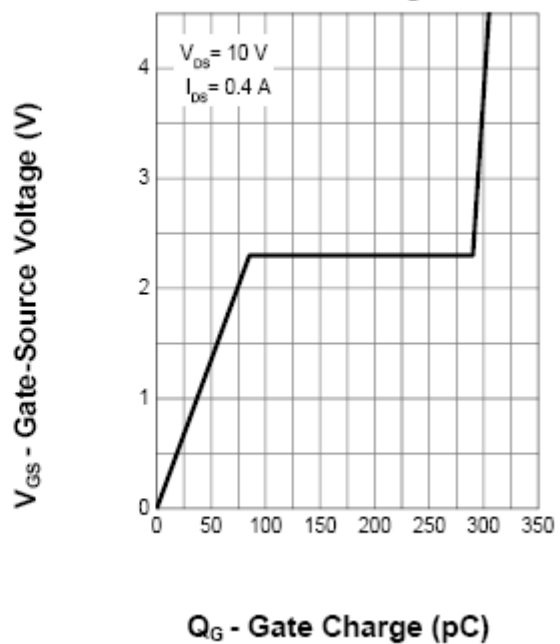
### Source-Drain Diode Forward



### Capacitance



### Gate Charge

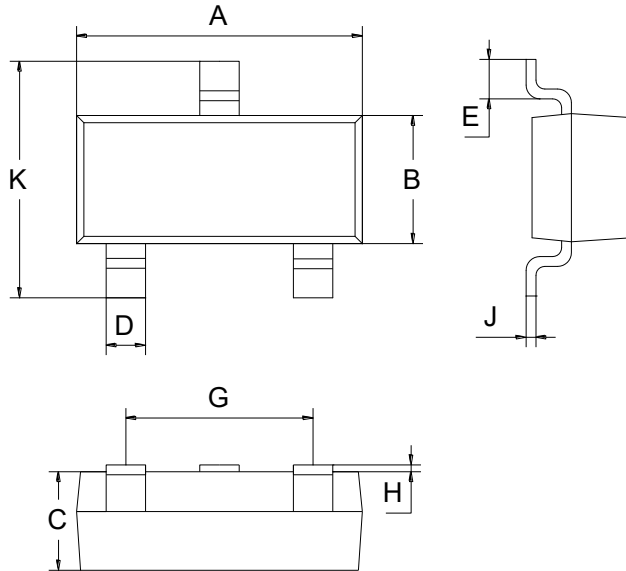




### PACKAGE OUTLINE

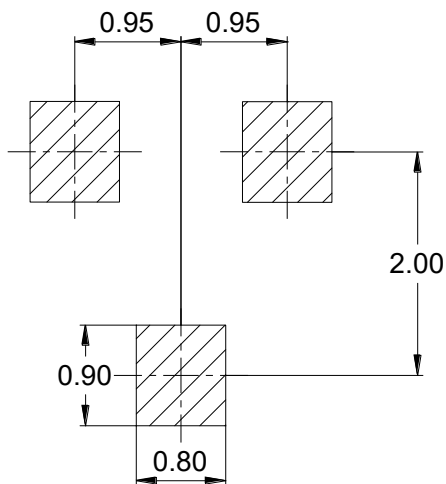
Plastic surface mounted package

SOT-23



SOT-23		
Dim	Min	Max
A	2.70	3.10
B	1.10	1.50
C	0.90	1.10
D	0.30	0.50
E	0.35	0.48
G	1.80	2.00
H	0.02	0.10
J	0.05	0.15
K	2.20	2.60
All Dimensions in mm		

### SOLDERING FOOTPRINT



Unit: mm

### PACKAGE INFORMATION

Device	Package	Shipping
LGE05N60C	SOT-23	3000 pcs / Tape & Reel